CLASS E SWITCHING MODE RF POWER AMPLIFIER

Jay Ellery Turner

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THESIS

CLASS E SWITCHING MODE RF POWER AMPLIFIER

by

Jay Ellery Turner

September 1977

Thesis Advisor: G. D. Ewing

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The class E switching mode rf power amplifier has many advantages over preveously developed power amplifiers. This thesis discusses the principles of operation, description, development, and performance of the amplifier along with laboratory test results.

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CLASS E SWITCHING MODE RF POWER AMPLIFIER

by

Jay Ellery Turner
Lieutenant, United States Navy
B.S., University of Utah, 1971

Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

The class E switching mode rf power amplifier has many advantages over preveously developed power amplifiers. This thesis discusses the principles of operation, description, development, and performance of the amplifier along with laboratory test results.

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I. INTRODUCTION

The term 'Power Amplifier' is used to refer to a circuit which produces a power output which is a significant part of its power input. A given device or combination of devices may often be used in a variety of ways to amplify a signal. The different modes of operation, or classes, can be defined in terms of how the devices are used. Classes A, B, and C refer to classical current source amplifiers. Class D and the relatively new class E are used to describe specific modes of high efficiency amplification.

In a high-efficiency power amplifier, increases of efficiency which at first might appear to be minor can be very important, e.g., increasing collector efficiency from 80% to 90% halves the collector power dissipation (reduction from 20% of the input power to 10%). That allows doubling the power output or halving the number of output devices and reducing the heat sink volume and weight. The recent large increases of energy cost provide futher incentive for reducing power losses in high-power fixed installations, and conservation of battery or generator power can be important for portable or remote equipment.

The major power loss is usually power dissipated in the output active device. To minimize that dissipation one attempts to minimize; 1) the voltage across the device when current flows through it, 2) the current through the device when voltage exist across it, 3) the duration of any unavoidable condition in which appreciable current and voltage exist simultaneously.

The following study consist of three sections which discuss how successful the different classes of power amplifiers are at accompolishing the formentioned minimization, with a focus on the class E switching mode rf power amplifier.

The first section is a review of classical current source amplifiers and introduces the switching mode amplifiers. In this section the collector efficiency of each amplifier is discussed and compared.

The second section is on the class E switching mode amplifier and discusses its principles of operation, circuit description, and the method for developing the circuit element values. The results of laboratory tests are also in this section as are some comments on recently developed VMOS devices which may have impact on switching mode amplifiers.

The last section consist of a brief summary of the characterstic advantages of the class E amplifier as well as concluding comments.

II. BACKROUND

A. CURRENT SOURCE AMPLIFIERS

1. Class A

In the class A amplifier the transistor current source is biased so that it conducts at all times. This bias current, which is modulated by the input signal, flows through the load impedance giving rise to an output voltage which is proportional to the input. Figure 1 shows a class A amplifier and fig. 2 shows the theoretical limiting case of maximum output. In order to approach this condition in practice the saturation resistance, Rs, of the transistor must be very small to make the collector voltage, Vc, approach zero while full peak current is flowing through it.

The maximum possible collector efficiency for a class A amplifier may be computed by solving for the average power dissipated in the transistor (Pd). For a sinewave input

$$Pd = \frac{1}{T}\int_0^T v_c\, i_c\, dt \qquad (1)$$

$$Pd = \frac{1}{T}\int_0^T V\left(1-\mathrm{SIN}\frac{2\pi}{T}t\right)I\left(1+\mathrm{SIN}\frac{2\pi}{T}t\right)dt$$

$$Pd = \frac{VI}{T}\int_0^T (1-SIN^2\frac{2\pi}{T}t)dt$$

$$Pd = \frac{VI}{T}\int_0^T \left(\frac{1}{2} + \frac{1}{2}COS\frac{4\pi}{T}t\right)dt$$

$$Pd = \frac{VI}{T}\left[\frac{1}{2}t + \frac{T}{8\pi}SIN\frac{4\pi}{T}t\right]_0^T$$

$$Pd = \frac{VI}{2}.$$

Since the dc collector input power is VccI, the maximum theoretical collector efficiency is 50% for the pure class A amplifier. In practice the overall efficiency is less than 50%.

Tuned circuits are not necessary for class A operation, and the amplifier is therefore capable of wideband (audio) amplification. The efficiency depends on the waveform being amplified. If a square wave is amplified (and the load is resistive) the efficiency can approach 100%. However, this is not true for most waveforms, and because of its inefficiency , class A is generally only used for low power amplifiers.

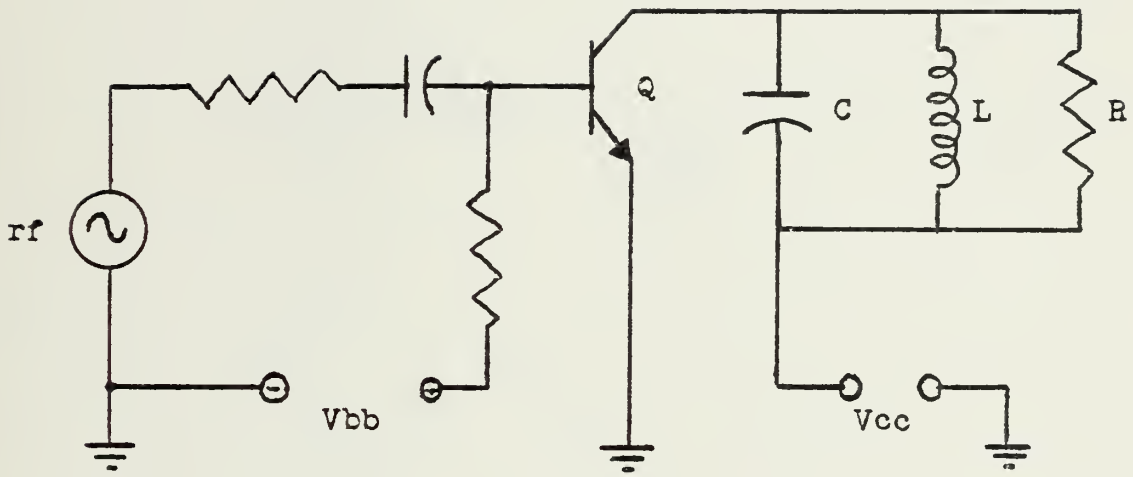


Figure 1 - CLASS A RF POWER AMPLIFIER.

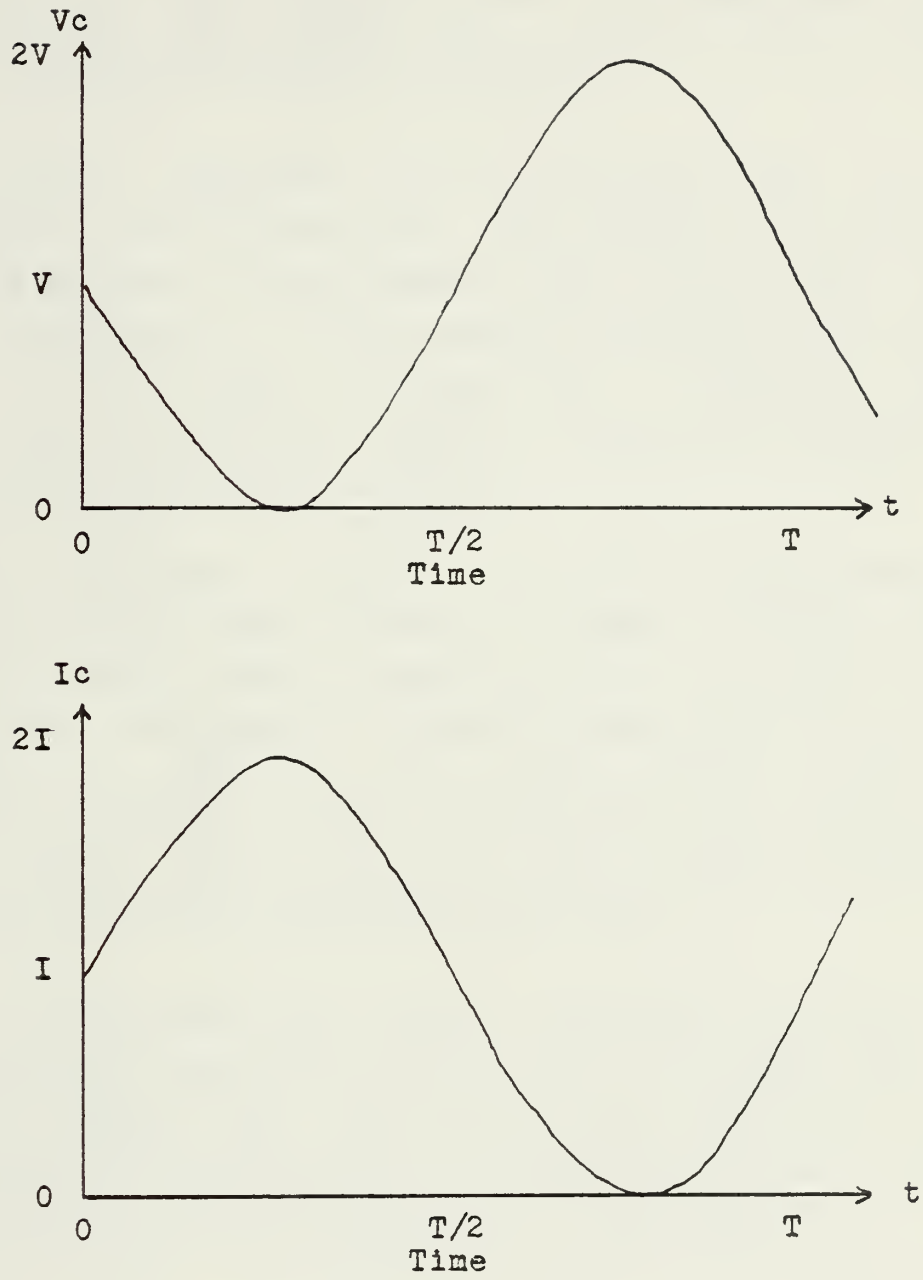


Figure 2 - THE THEORETICAL LIMITING CASE OF MAXIMUM OUTPUT FOR THE CLASS A RF AMPLIFIER.

2. Class B

Class B operation makes possible linear amplification with improved efficiency. Both single-ended tuned versions and push-pull broad band versions are possible.

In class B operation, the transistor acts as a current source half of the time. The current is zero when the collector voltage is the highest, which contributes to the higher efficiency. In the push-pull configuration, one transistor or the other is always on, creating the equivalent of a continuous current source and therefore making wideband amplification possible.

The collector current in the single-ended configuration is a half sinewave. Figure 3 shows the theoretical maximum output condition for the class B rf power amplifier. The parallel resonant tuned circuit has a low impedance to harmonics, and passes them to ground. Since almost no harmonic voltage is generated, the collector lead will supply a good sinusoidal output voltage provided the Q of the circuit is reasonably high, Q=10.

As in the case of the class A amplifier the class B amplifiers maximum collector efficiency may be calculated by computing the average power dissipated in the transistor for the limiting case of zero saturation voltage occuring at the instant of peak collector current flow. From equation 1

$$Pd = \frac{1}{T}\int_0^T v_c\, i_c\, dt$$

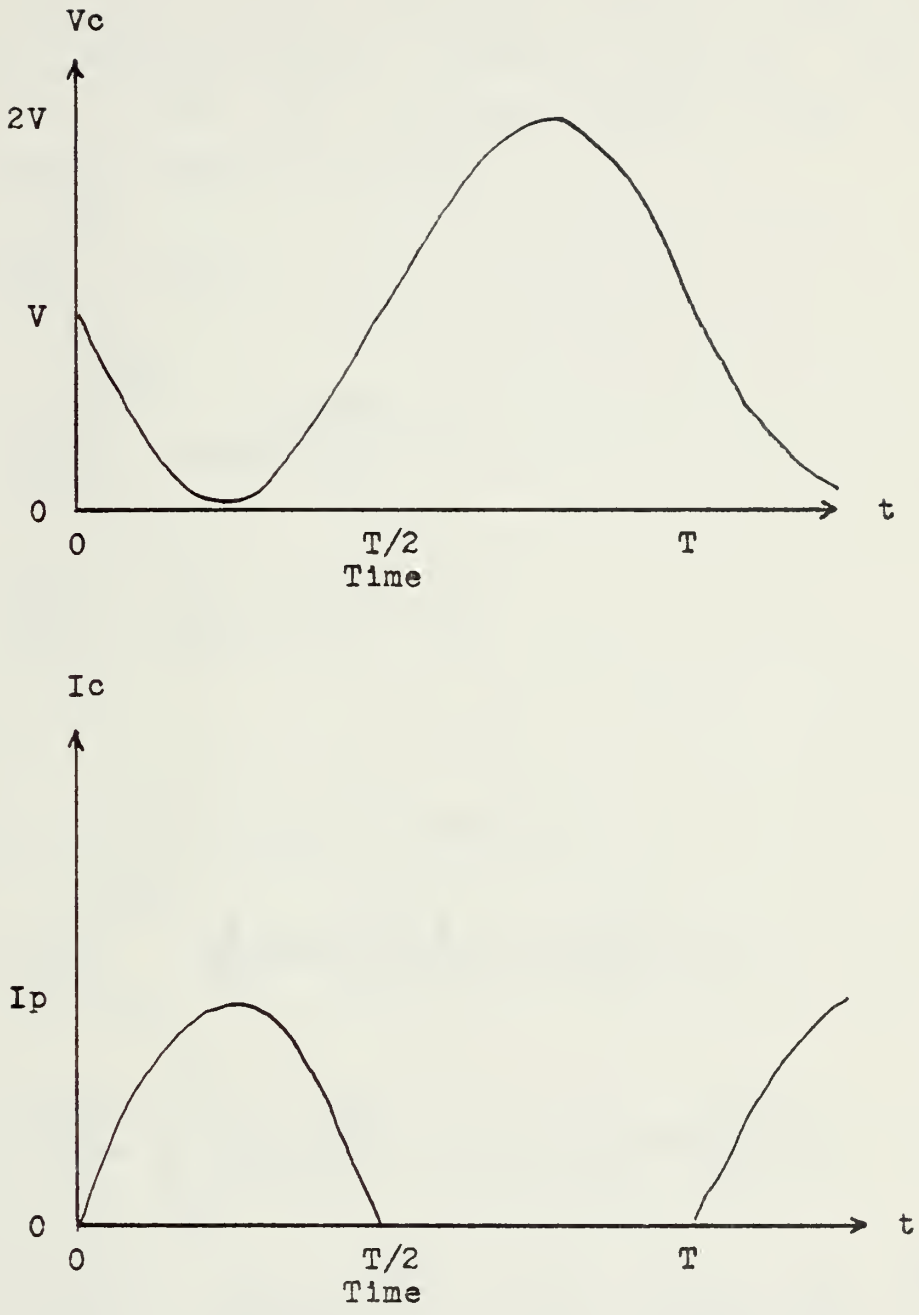


Figure 3 - THE THEORETICAL LIMITING CASE OF MAXIMUM OUTPUT FOR THE CLASS B RF AMPLIFIER.

It is necessary to establish the peak current Ip flowing through the transistor as a function of the average dc current supplied to the collector circuit in order to evaluate the theoretical maximum collector efficiency. This is easy to do since the collector current flows in sinusoidal pulses as shown in fig. 3.

$$I = \frac{1}{T}\int_0^T i_c \, dt$$

$$I = \frac{1}{T}\int_0^{T/2} Ip \, SIN\frac{2\pi}{T}t \, dt$$

$$I = \frac{Ip}{T}\left[-\frac{T}{2\pi}COS\frac{2\pi}{T}t \right]_0^{T/2}$$

$$Ip = \pi I$$

Now the expression for Pd may be evaluated.

$$Pd = \frac{1}{T}\int_0^{T/2} V\left(1-SIN\frac{2\pi}{T}t\right)\pi I \, SIN\frac{2\pi}{T}t \, dt$$

$$Pd = \frac{\pi VI}{T}\int_0^{T/2}\left(SIN\frac{2\pi}{T}t - \frac{1}{2} + \frac{1}{2}COS\frac{4\pi}{T}t\right)dt$$

$$Pd = \frac{\pi VI}{T}\left[-\frac{T}{2\pi}COS\frac{2\pi}{T}t - \frac{1}{2}t + \frac{1}{8\pi}SIN\frac{4\pi}{T}t \right]_0^{T/2}$$

$$Pd = \frac{\pi VI}{T}\left(\frac{T}{2\pi} + \frac{T}{2\pi} - \frac{T}{4} \right)$$

$$Pd = \pi VI\left(\frac{1}{\pi} - \frac{1}{4}\right)$$

$$Pd = VI\left(1 - \frac{\pi}{4}\right) \qquad (2)$$

Since the dc input power to the collector circuit is VccI, the power available at the load is $\frac{\pi}{4}$VccI as evident from equation 2. The efficiency attained in practice is much lower than this value due to finite transistor on resistance.

Amplification of different waveforms results in different efficiencies. If the load of a push-pull class B amplifier is a pair of diodes or transistor bases, a square wave collector voltage will result, and the efficiency can approach 100% with the optimum transformer. The output does not depend on the collector supply voltage as long as the amplifier is not saturated. Variations of the supply voltage do nct modulate the output, although they do change efficiency.

The tuned class B power amplifier affords the highest overall efficiency of the linear class of amplifiers. It is used in the high level stages of rf transmitters where reasonable linearity and efficiency are prerequisite.

3. Class C

Class C operation is simular to single-ended class B

operation. The difference is that the transistor is biased to operate as a current source less than half of the time. The result is that the collector current flows near the minimum cclllector voltage, resulting in a higher efficiency. However, the input-output characterstics are no longer linear.

Figure 4 shows the collector voltage and current waveforms of a pulse excited class C amplifier. To find an expression for collector efficiency, equation 1 is applied

$$Pd = \frac{1}{T}\int_{-t_1/2}^{t_1/2}\left[V - (V - Vs)COS\frac{2\pi}{T}t\right]Ip\ dt$$

$$Pd = \frac{Ip}{T}\left[Vt - \frac{T}{2\pi}(V - Vs)SIN\frac{2\pi}{T}t\right]_{-t_1/2}^{t_1/2}$$

$$Pd = \frac{Ip}{T}\left[Vt_1 - \frac{T}{\pi}(V - Vs)SIN\frac{\pi t_1}{T}\right]$$

Vs is defined as the saturation voltage of the transistor with Ip flowing through it. Since the saturation resistance ($Rs=\frac{Vs}{Ip}$) of the transistor is dependent on voltage, current, and temperature, the following equations are close approximations.

Appling equation 2 results in

$$I = \frac{1}{T}\int_{-t_1/2}^{t_1/2} Ip\ dt \qquad = Ip\frac{t_1}{T}$$

Solving for Ip and substituting into the expression for Pd yields

$$Pd = I\left[V - \frac{T}{\pi t_1}(V - Vs)SIN\frac{\pi t_1}{T}\right]$$

$$Pd = VI\left[1 - \frac{T}{\pi t_1}(1 - \frac{Vs}{V})SIN\frac{\pi t_1}{T}\right] \qquad (3)$$

Thus the collector efficiency is dependent upon the conduction angle and the ratio of the saturation voltage to the dc supply voltage.

Since the saturation voltage Vs is dependent to a first approximation linearly on the collector peak current Ip, equation 3 may be written

$$eff. = \frac{T}{\pi t_1}(1 - \frac{RsIp}{V})SIN\frac{\pi t_1}{T}$$

For any given transistor Rs is fixed and the collector current Ip is limited.

The practical efficiency of a class C rf power amplifier is significantly higher than even the theoretical maximum efficiency of a class B rf power amplifier.

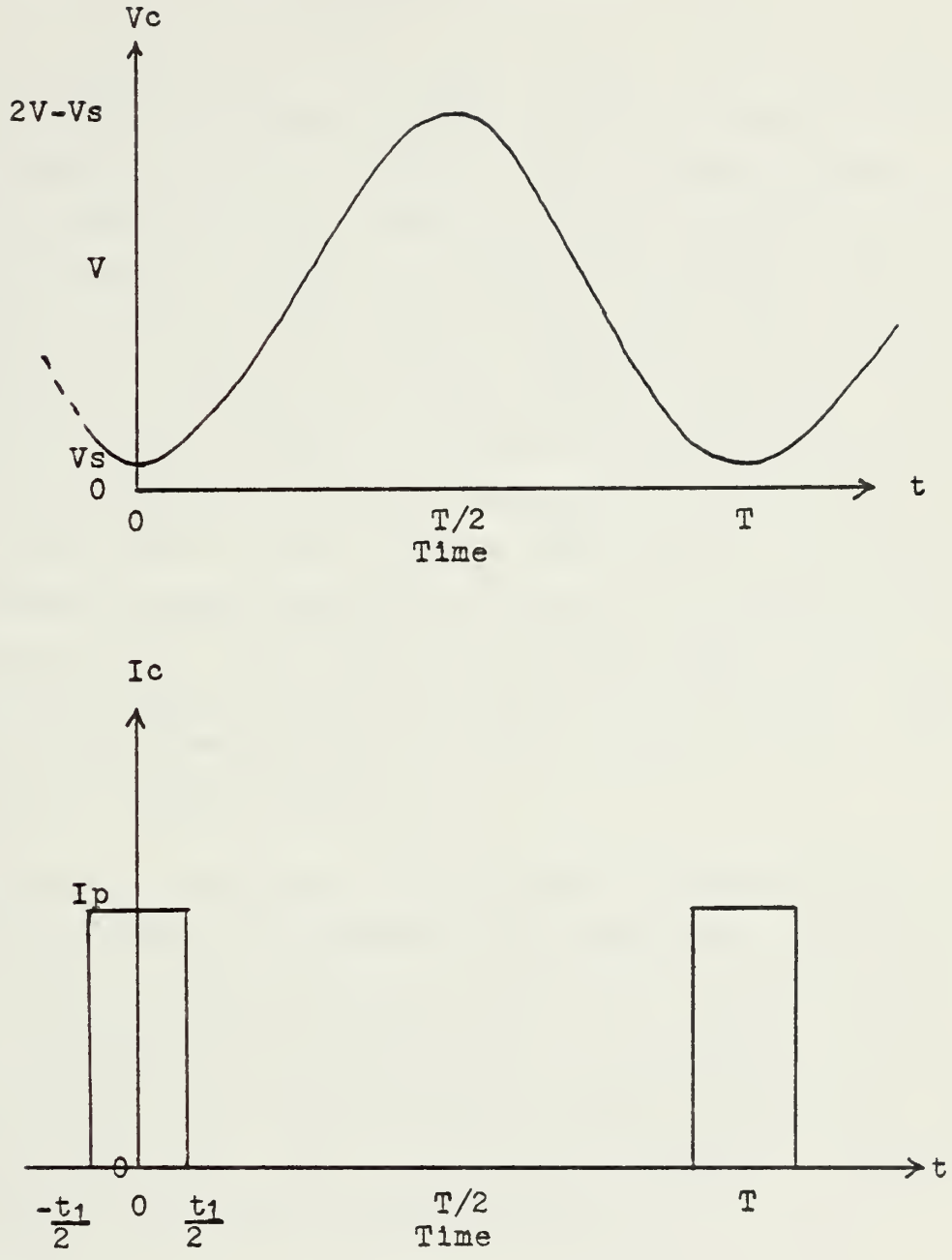


Figure 4 - CLASS C RF POWER AMPLIFIER COLLECTOR VOLTAGE AND CURRENT VS TIME.

4. Summary of Current Source Amplifiers

In designing a tuned class C rf power amplifier,[1]-[8], the output active device is assumed to be a high-impedance current source. Its output current is determined primarily by the input drive and is substantially independent of the output voltage which results from the flow of that current in the load network. The load network is designed so that its voltage response to the periodic current pulses is a sinusoid at the output frequency. The properties of this design are that the minimum collector voltage occurs across the current source at the time of the current pulse and, at this minimum, the voltage is not less than a certain minimum permissible voltage determined by the characterstics of the active device and required for the device to function as a current source as assumed. This voltage prevents "saturation" of the transistor which would invalidate the design assumption.

Harmonic resonators can be added to the load network to improve the trade-off between efficiency and conduction angle. This provides approximately a flat-bottomed voltage waveform when the network is driven by the pulsed current source, extending the duration of the low-voltage condition and permitting a wider current pulse without severe loss of efficiency, [9]-[11]. This circuit also requires a minimum voltage across the current source device.

All current source amplifiers dissipate substantial power in the active device because the voltage across that device during the current pulse must be larger than the minimum permissible value. Obtaining high efficiency requires that the current pulse amplitude and the load network be adjusted carefully to obtain an ac output voltage

amplitude which is large enough to bring the active device voltage as close to zero as allowable during the current pulse, but not so large as to cause the device voltage to become less than the minimum permissable voltage thereby causing the device to be no longer a high-impedance current source and invalidate design assumptions.

B. SWITCHING AMPLIFIERS

1. Class D

A class D rf power amplifier,|12|-|15|, employs a pair of transistors which are driven to act as a two position switch and a tuned circuit or bandpass filter. The switch is always in one position or the other, and hence determines either a voltage or current waveform.

Figure 5 is the complimentary configuration of a class D amplifier. The input of the tuned circuit is alternately connected to Vcc and ground, and has a square voltage waveform. The series-tuned circuit has zero impedance to the fundamental switching frequency, allowing the fundamental frequency component of the square wave to appear on the load. The current generated is sinusoidal, and alternate half cycles flow through alternate transistors. When current is flowing in a given transistor, the voltage across it is (ideally) zero, making an efficiency of 100% (ideally) possible. The high impedance of the series-tuner circuit at harmonic frequencies prevents harmonic current and power from being generated.

A variation of the class D amplifier is the current switching configuration (fig.6). The rf choke forces an

essentially constant input current. The transistors are driven on and off alternately, as before. Since one or the other conducts all of the dc input current , the collector currents are square waves. The parallel-tuned output circuit bypasses the harmonics contained in the square wave, allowing only the fundamental frequency component to reach the load. The parallel-tuned circuit forces the output voltage, and hence the voltage on the transformer primary, to be sinusoidal. When one of the transistors is on, its collector voltage is zero, so the collector voltage of the other transistor must be sinusoidal. The result is a collector voltage which is half a sinusoid. Dc balance requires that the peak collector voltage be Vcc. Although voltage balance determines the power output, this amplifier is like a current source, and therefore requires a parallel-tuned circuit or a bandpass filter which has a low impedance to the harmonic frequencies.

While 100% efficiency is theoretically possible, real devices have non-zero saturation voltage and non-instantaneous switching times. Bipolar transistors are characterized by a nearly constant saturation voltage which is equivalent to an unwanted drop in the supply voltage. FET's are characterized by a nearly constant saturation resistance which is equivalent to an unwanted addition to the load resistance. The decrease in efficiency which results is simply proportional to the ratio of saturation voltage to supply voltage or saturation resistance to load resistance. This same loss of efficiency was also observed in class B amplifiers.

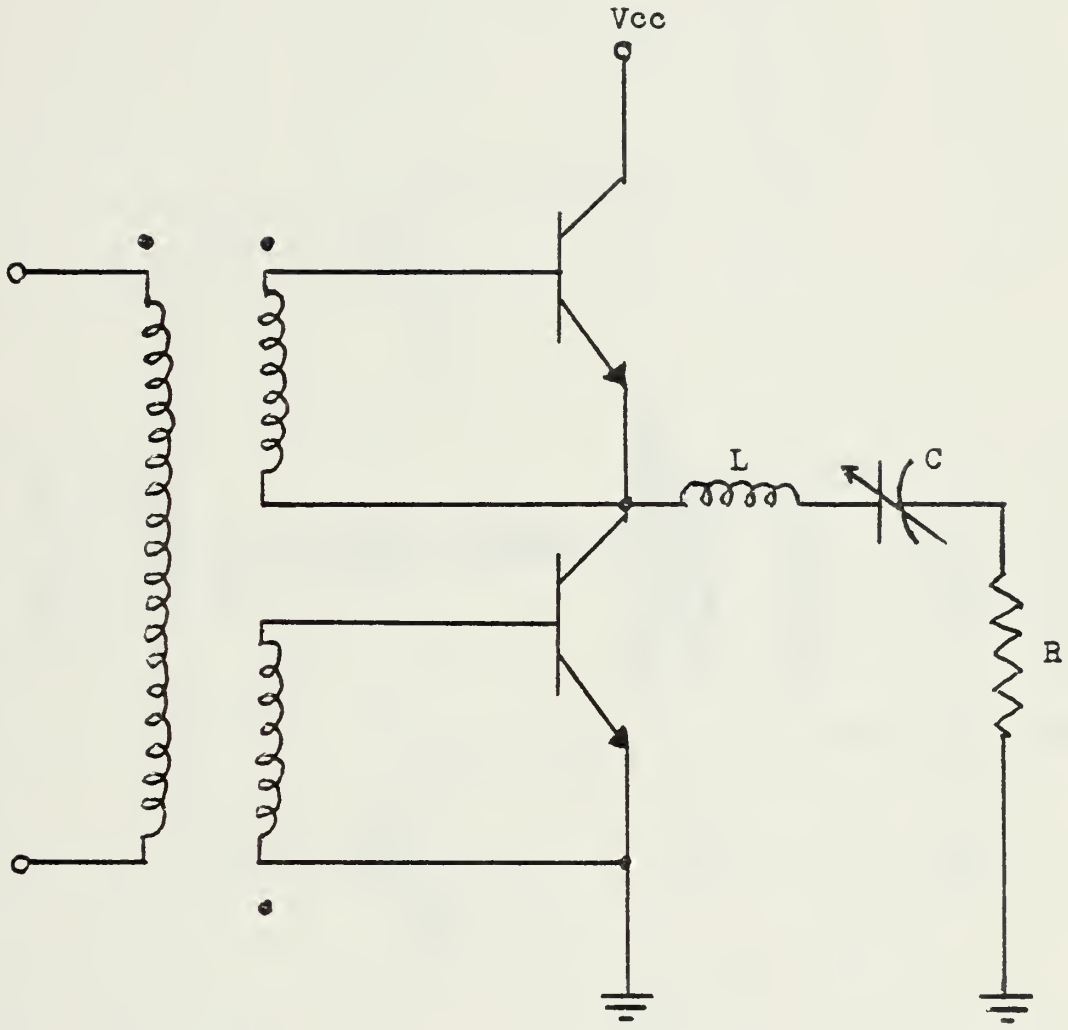


Figure 5 - COMPLIMENTARY CLASS D RF POWER AMPLIFIER.

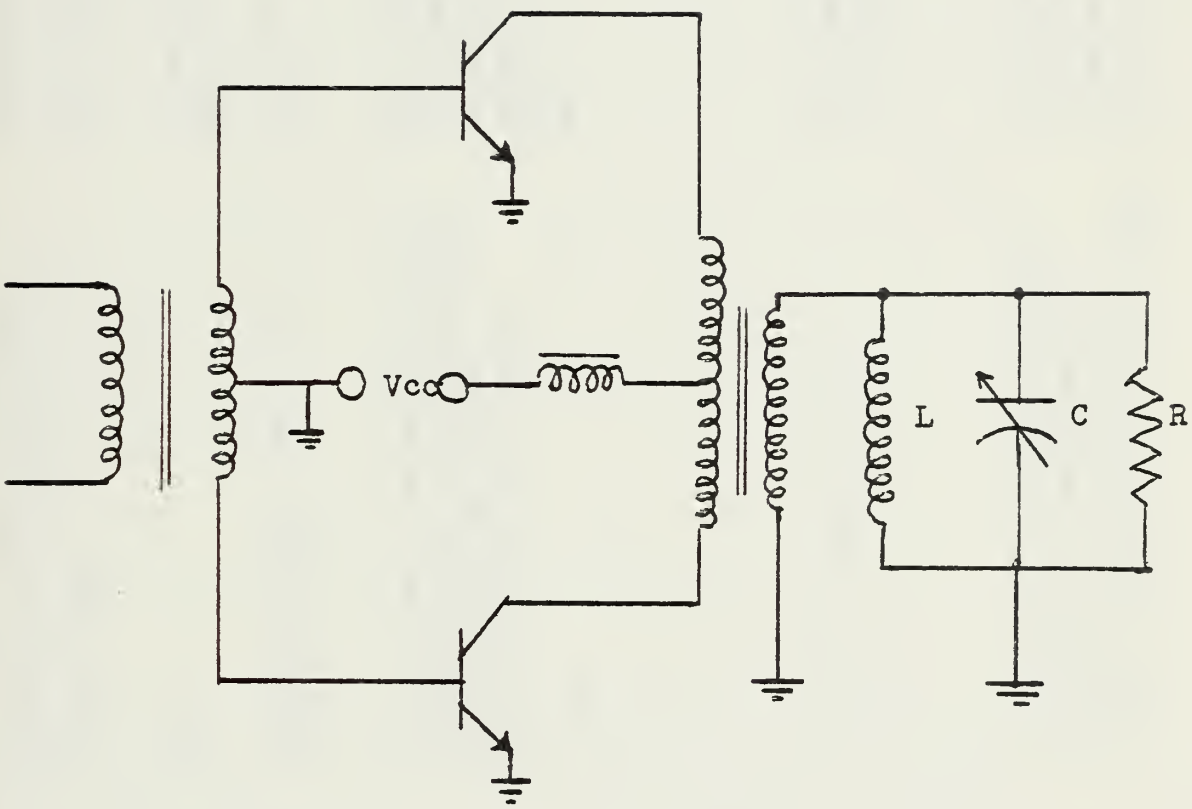


Figure 6 - CURRENT SWITCHING CLASS D RF POWER AMPLIFIER.

CHARACTERSTIC	CURRENT SOURCE AMPLIFIER	SWITCHING AMPLIFIER
Active device output-port ac impedance.	Always high.	'on' low. 'off' high.
Is the active device allowed to saturate.	No.	Often intentionally when on.
Desired voltage across the active device when conducting current.	Greater than a specified minimum value.	As low as can be obtained.
What determines the voltage across the active device while its conducting.	The voltage response of the load network input impedance to the current pulses delivered by the source.	The voltage approaches zero because of the low-impedance property of the switch, independent of the load.
Does the voltage across the active device output-port during the current conduction depend on the load network input port impedance.	Yes.	No.
What determines the current which flows through the active device when its conducting current.	Only its input signal.	The load network to which its output is connected.
To what criteria should the load network be designed.	The input voltage waveform produced in response to a specified current-pulse train injected into its input.	The input voltage waveform produced by repetitive alternatively connected short and open circuits at its input.

Table 1 - USE OF CURRENT SOURCE AMPLIFIER VS SWITCHING AMPLIFIER.

Collector modulation of a class D amplifier is very linear, |16|. There is no saturation angle which can vary, as in the class C amplifier. There are two sources of non-linearity which occur at near-zero collector voltage. One is due to the deterioration of the constant saturation voltage characterstic as Vcc approaches Vsat. The other is drive feedthrough from Cob. While the saturation voltage merely tends to make a slightly non-linear transfer curve, the drive feedthrough sets a lower limit on the output. Both effects are generally small. Efficiency also decreases as the collector voltage is reduced, but remains higher than that of a class B or C amplifier with reduced output.

The class D amplifiers are efficient, but suffer from the possibility of both transistors conducting simultaneously or being off simultaneously during the switching transient, leading to loss of efficiency at high frequencies and to the possibility of transistor destruction by second breakdown, |12|.

2. Summary of Switching Amplifiers

High efficiency can be achieved by using the active device as an on/off switch instead of a high-impedance current source. The increased efficiency results from reducing the voltage which exist across the device while current is flowing through it. While a practical active-device current source requires at least a certain minimum permissible voltage across itself, an active device switch may be operated at a much smaller "on" voltage. Table I shows the fundamental differences between the use of a current source to drive a load network and the use of a switch to drive a differently designed load network to be described in the following section.

III. THE CLASS E SWITCHING MODE RF POWER AMPLIFIER

A. PRINCIPLES OF OPERATION

Figure 7 is a block diagram of a single-ended switching mode amplifier. The active device output is represented as a nonideal single-pole single-throw switch; the 'on' resistance may be non-zero, the 'off' resistance may be non-infinite, and the turnon and turnoff switching time may be non-zero. As the switch is operated at the desired ac output frequency, dc energy from the power supply is converted tc ac energy at the switching frequency (and harmonics thereof). To obtain maximum fundamental-frequency output, the switch duty ratio is made approximately 50%, (18). The load network may include a lowpass or bandpass filter to suppress harmonics of the switching frequency at the load, and may transform the load impedance and/or accomodate load reactance.

Figure 8 shows the desired waveforms of voltage across the switch and current through the switch, in a circuit of the fig. 7 class arranged for maximum power efficiency. The following conditions are met by those waveforms: 1) the voltage across the switch when current flows through it is very low; 2) the current through the switch when voltage is across it is zero; 3) the switching time of the switch is minimized. These three conditions are accompolished by proper choice of the switching device and the excitation circuit.

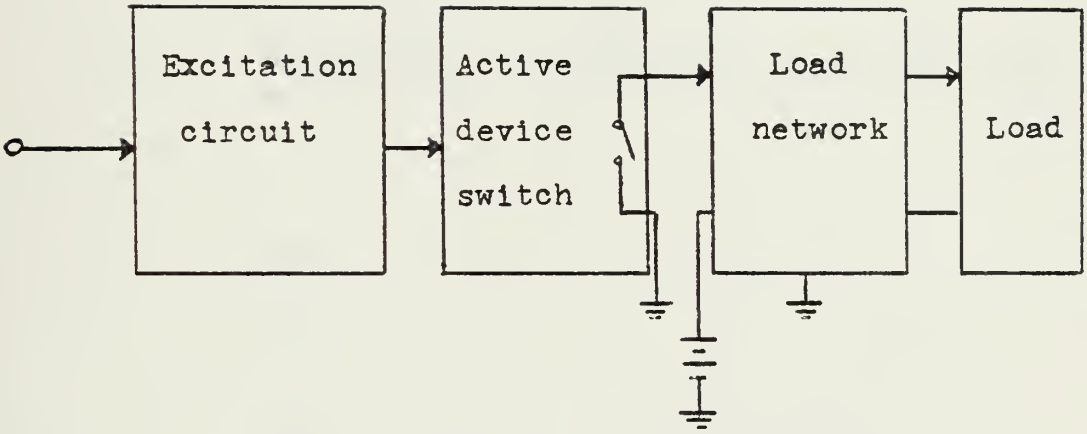


Figure 7 - BLOCK DIAGRAM OF A SINGLE-ENDED SWITCHING - MODE AMPLIFIER.

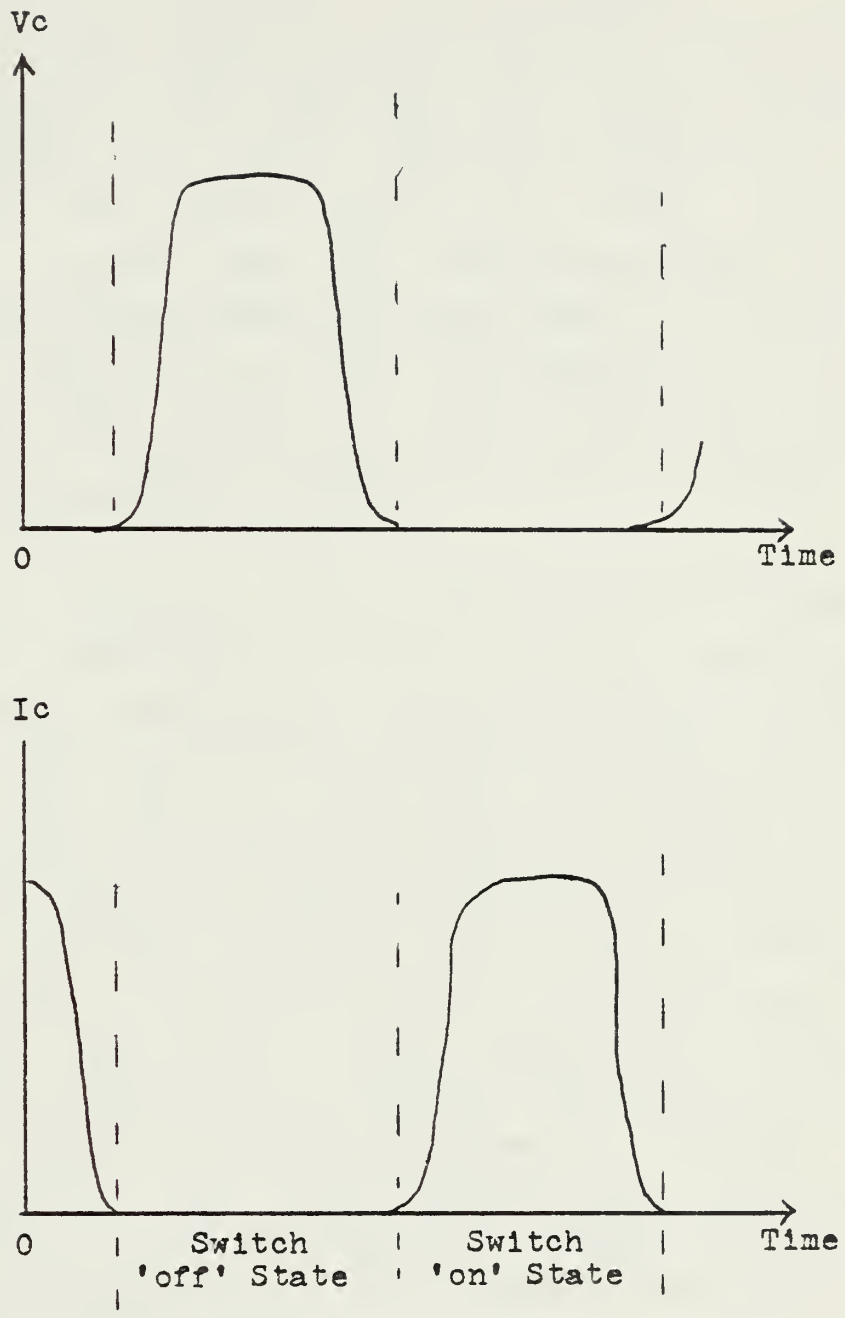


Figure 8 - OPTIMUM WAVEFORMS IN CIRCUIT OF FIG. 7 ARRANGED FOR MAXIMUM POWER EFFICIENCY.

The load network is arranged to have the input-port transient response described in conditions 4) through 6).

Condition 4) Voltage delay at switch turnoff; in the time interval during which the switch makes its transition from the 'on' state to the 'off' state, the voltage across the switch remains low for a time long enough that the current through the switch has by then been reduced substantially to zero. Then the voltage increases. This assures that high voltage does not exist across the switch while current through it is non-zero, avoiding the energy loss which would have existed if the voltage had been allowed to start to increase before the current decrease to zero had been substantially completed.

Condition 5) Voltage return to zero at switch turnon; during the switch 'off' state, the load network input-port transient response carries the voltage across the switch first upwards, and then downwards toward zero, this voltage reaches zero just prior to the start of the switch 'on' state. This aviods the energy dissipation which would have occured if the switch current had begun flowing while the voltage across the switch was still high, and had thereafter discharged tc ground, through the switch, the capacitance at the load network input port. This capacitance includes intrinsic switch capacitance and circuit stray capacitance, as well as any capacitor purposely designed to be part of the tuned circuit. Each time a capacitance C, initially charged tc a voltage V, is discharged by a switch, an energy $CV^2/2$ will be dissipated. This causes a power loss of $CV^2f/2$, reducing efficiency.

Condition 6) Zero voltage slope at switch turnon; when the 'off' state transient response reaches zero voltage across the switch it does so with approximately zero slope ($dv/dt=0$). This permits slight mistuning of the amplifier

without severe loss of efficiency because there is a time interval during which the switch turnon can occur while still substantially meeting the condition of v=0. Moderately slow turnon of the switch does not cause the switch to experience high power dissipation during turnon because the voltage across the switch is not increasing rapidly during the time that the switch is turning on.

The conditions v=0 and dv/dt=0 at the end of the 'off' state imply that the current at the start of the 'on' state will be zero, and that during the 'on' state the switch current can gradually increase from zero. Because of the limited di/dt capabilities of real active-device switches, this zero starting current is desirable because it helps minimize switch turnon time and further minimize dissipation during the turnon transient.

The waveforms of fig. 8 can only be accompolished by appropriate design of a non-resistive load network, and results in a considerable increase in efficiency if the transition time of the switch is an appreciable fraction of a half-cycle of the ac waveform.

B. CIRCUIT DESCRIPTION

The preveous principles will now be illustrated by the circuit shown in fig. 9. This circuit was orginally developed and analyzed by Ewing [17] in 1964 for his Ph.D. thesis at Oregon State University. This circuit was also analyzed and published by Sokal [18] in 1975 (although Sokal did present a preliminary version at the 1972 IEEE International Symposium on Circuit Theory in Los Angeles).

L1 is a high-reactance Vcc shunt-fed rf choke, large

enough to act as a source of constant current. The sum of its shunt capacitance, the transistor output capacitance, and wiring capacitance is absorbed into C1. R may be the actual load, or may be the input-port resistance of a low pass filter inserted between the C2-L2 branch and the load to suppress harmonics of the switching frequency.

In the class E amplifier circuit the collector voltage is at Vce(sat) while the transistor is on, satisfying condition 1 of the preveous discussion. When the transistor is switched off, the load network transient response is the response of a damped second order system, the series connection of L2, R, and C1C2/C1+C2, starting with some initial condition. Some of the energy stored in C1 C2 and L2 is delivered to R during the ringing transient.

C1 insures that in the time interval during which the transistor is being turned off, Vce remains relatively low until after the collector current has reduced to zero, approximating the delay of voltage rise shown in fig. 8 and discussed preveously as condition 4. High Vce does not occur until after Ic has been cut off at low voltage and the base has become reverse biased. Thus the BVcev rating applies to the 'off' condition, rather than the lower BVceo or BVcer ratings. This allows using a higher value of Vcc, thereby obtaining higher power output and higher efficiency.

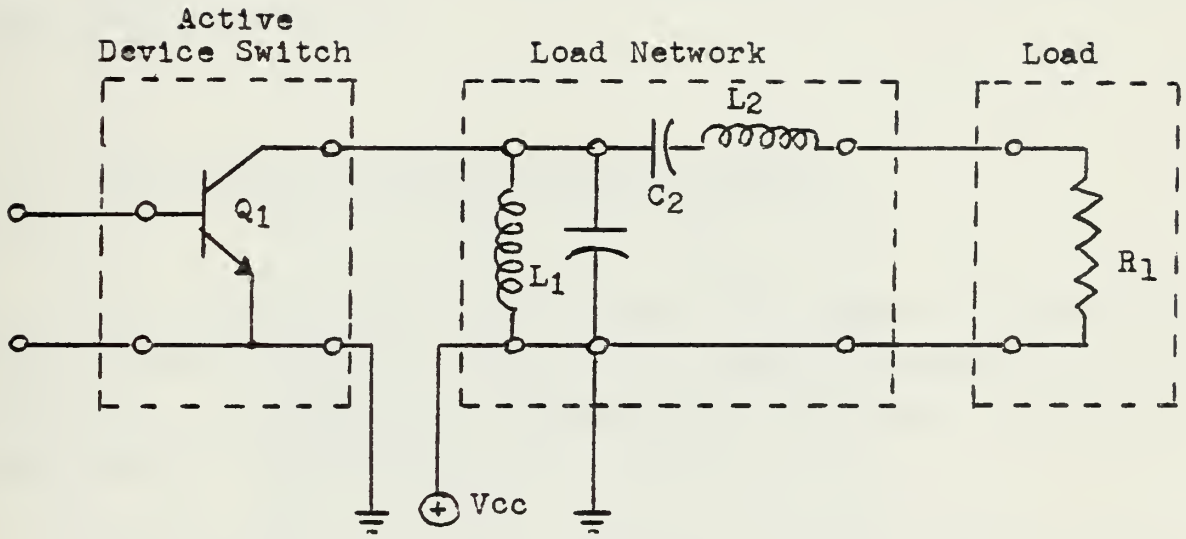


Figure 9 - CIRCUIT DIAGRAM OF THE CLASS E RF POWER AMPLIFIER.

The waveforms of fig. 10 show the three types of transient responses for three different values of damping corresponding to three different values of load network Q (Q1). The Q1 to low case is shown in fig. 10 (a), the voltage across C1 never returns to zero, causing unwanted power dissipation. The Q1 to high case is shown in fig. 10 (b), Vce swings below zero placing the transistor in the inverted mode. This can cause unwanted power dissipation and/or transistor damage. The Q1 correct case is shown in fig. 10 (c), the peak negative-going Vce just reaches Vce(sat) (=0). The correct damping also gives zero slope to the Vce waveform as it reaches the zero value at the end of the 'off' half-cycle.

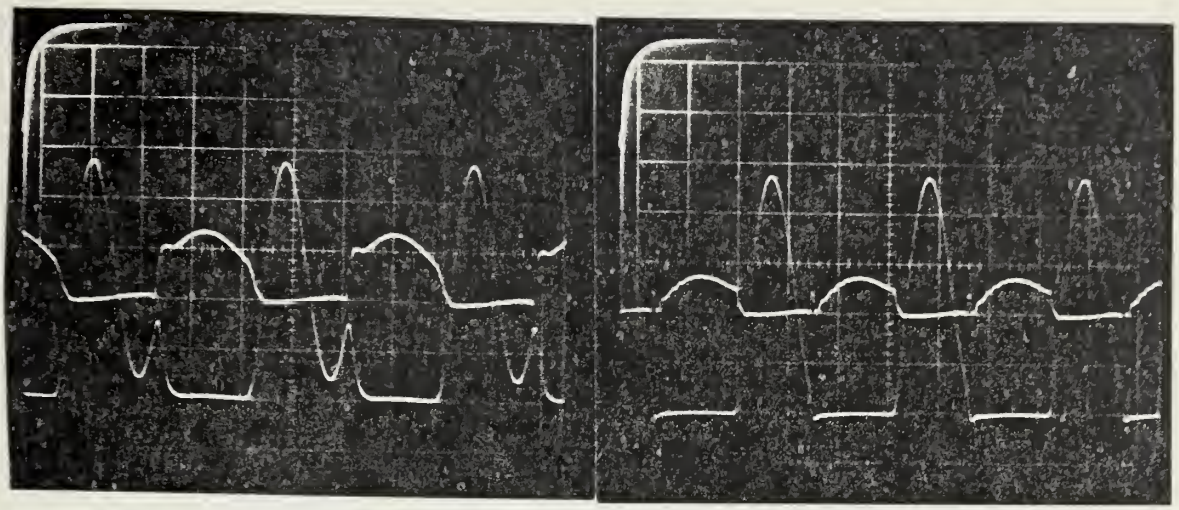
C. DEVELOPMENT OF CIRCUIT ELEMENT VALUES

The element values for the class E rf power amplifier of fig. 9 are obtained by choosing the three variables C1, C2, and L2 to meet simultaneously the three following mathematical conditions, |17|-|18|.

Condition 1: Vce=0 at t=(1-d)(1/f) after switch turnoff time, where f is the operating frequency and d is the switch duty ratio, here taken as 50%.

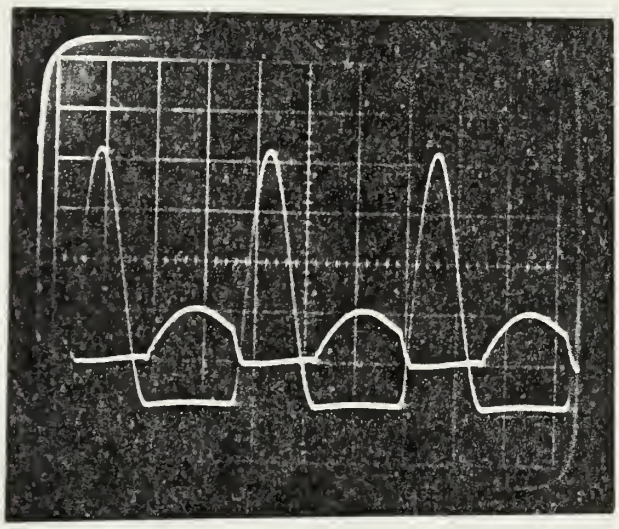
Condition 2: dVce/dt=0 at t=(1-d)(1/f) after switch turnoff time.

Condition 3: Q1 is any chosen value.



(a) Q_1 to low.

(b) Q_1 to high.



(c) Q_1 correct.

Figure 10 - TRANSIENT RESPONSES FOR THREE DIFFERENT VALUES OF LOADED Q. Upper trace is collector current and lower trace is collector voltage. Scale settings: Ic .5 a/div.; Vc 10 v/div.; horizontal, .25 usec./div.

A specific C1/C2 ratio makes that chosen Q1 provide the proper damping shown in the 'Q1 correct' curve of fig. 10, yielding the zero-slope zero-value Vce at turnon time. Equations will now be given for the element values of the circuit in fig. 9. The equations have been derived by Ewing |17| and are for a 50% duty ratio.

The values of R and Vcc are constrained by the requirement to deliver a specified power output to the load from the Vcc power supply; specifying either one dictates the other. For highest efficiency, the highest possible Vcc should be used, within the Vce limitation of the transistor. The value of R is found as

$$R = \frac{(Vcc - Vce(sat))^2}{P} \left(\frac{2}{\frac{\pi^2}{4} + 1} \right)$$

$$R = .577 \frac{(Vcc - Vce(sat))^2}{P}$$

Impedance transformation can be used if the load resistance is not equal to this value of R. The desired Q1 may be chosen freely, according to the design compromise to be made between efficiency and harmonic content of the power delivered to the load , |18|. Then

$$L_2 = Q_1 R/2\pi f$$

To satisify the conditions Vce=0 and dVce/dt=0 at t=0.5/f after switch turnoff, given the chosen Q1,

$$C_2 = 1/2\pi fR \left(\frac{\pi^2}{4} + 1 \right)\left(\frac{\pi}{2} \right)$$

$$C_2 = 1/2\pi fR \ (5.447)$$

and

$$C_1 = \left(\frac{1}{(2\pi f)^2 L_2}\right)\left(1 + \frac{1.42}{Q_1 - 2.08}\right)$$

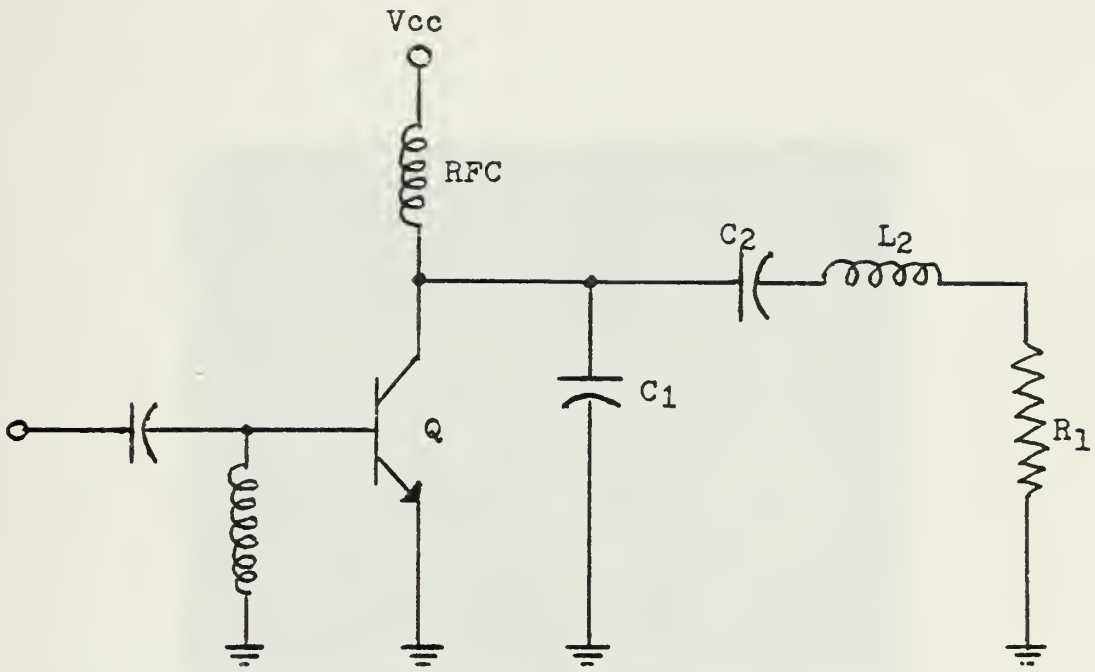
$$C_1 = C_2\left(\frac{5.447}{Q_1}\right)\left(1 + \frac{1.42}{Q_1 - 2.08}\right)$$

Note that L2 is not resonant at f with C1 or with the series combination of C1 and C2. Load reactance (if any) is accommodated by absorbing it into C2 and L2: the inductance of L2 is decreased if the load series reactance is inductive, the capacitance of C2 is increased if the load reactance is capacitive, or both are done if the load is a combination of inductance and capacitance.

D. LABORATORY RESULTS

The class E rf power amplifier of the type in fig. 9 was built and tested under laboratory conditions. The circuit model with its component values are shown in fig. 11. These component values were obtained from the design method preveously discussed. Figure 12 shows an oscillogram taken from a Tektronix type 422 oscilloscope equipped with a dual trace feature having 10 megohm-10 picofarad probes. The peak load voltage V1 is found to be 11.5 volts. The peak collector voltage across Q1 is 42 volts which is below the BVce of about 60 volts. The measured dc current with 12 volts Vcc was 150 milliamperes, giving the total dc input power of 1.8 watts. The power dissipated in the rf choke is given by

$$Prfc = (.15)^2\ (5.5) \qquad = .124 \text{ watts}$$



Q = 2N3118
L_2 = 92 - 187 microhenry; .3 ohm
C_1 = 1300 picofarad
C_2 = 2200 picofarad
R_1 = 42 ohms
f = 500 khz.
Vcc = 12 volts
RFC = 3 millihenry; 5.5 ohm

Figure 11 - MODEL CLASS E SWITCHING MODE RF AMPLIFIER.

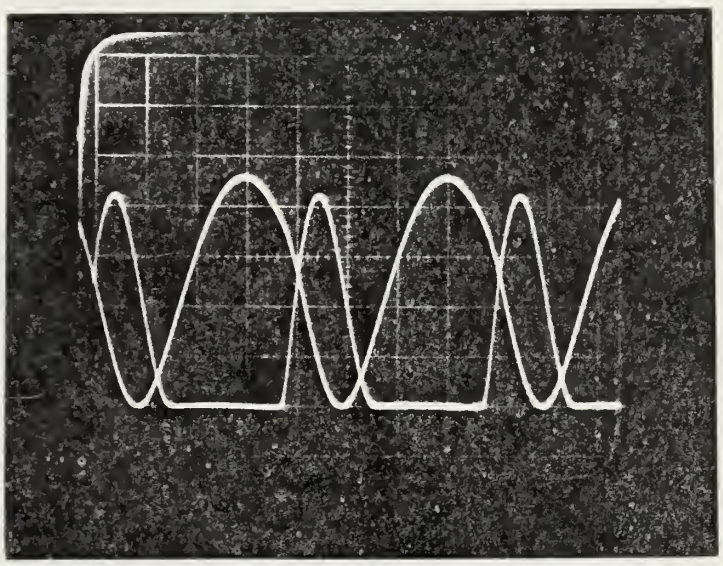


Figure 12 - LOAD AND COLLECTOR VOLTAGE OF THE CLASS E RF POWER AMPLIFIER. Sinusoid is output voltage. Scale settings: Vc 10 v/div.; Vo 5 v/div. Horizontal .5 usec./div.

Therefore, the actual input power to the collector circuit is 1.676 watts. The peak load current Il is

$$I_1 = \frac{11.5}{42} = .274 \text{ amperes}$$

The ac power delivered to the load Pl is

$$P_1 = \frac{V_1 I_1}{2} = \frac{(11.5)(.274)}{2} = 1.576$$

Neglecting the power lost in the distributed resistance if inductor L2 and the capacitors C1, and C2, the collector efficiency of the amplifier is calculated to be approximately

$$\text{eff.} = \frac{1.576}{1.676} = .94 \text{ or } 94\%$$

Now approximately 3% of the collector power is absorbed in L2, C1, and C2. Therefore the collector efficiency of the tuned class E amplifier as described is approximately 97%.

1. Circuit Excitation

To increase overall stage efficiency a high input impedance exciter circuit should be used. For the amplifier to be excited by a sinusoidal input voltage, which is the most easily obtained waveform, the exciter device should be an enhancement mode FET with high transconductance and have output characterstics giving a steep-edged drain current waveform for about 180 degrees of the input signal cycle.

2. Detuning Effects

Table II shows how the collector efficiency is affected by varying the input excitation frequency of the circuit in fig. 11. The dc supply voltage was held at 12 volts as before along with all circuit parameters.

The input excitation frequency can vary from approximately -8% to +12% of the tuned frequency without the collector efficiency dropping below 90%. As the frequency is decreased below -8% the efficiency drops off rapidly, this not true with an increase of frequency above +12%, in which case the collector efficiency drops rather slowly.

Table II also shows that tuning the amplifier for maximum power output does not correspond to the condition of maximum efficiency. The maximum power out occurs when the excitation frequency is approximately 6% to 7% below the tuned frequency. The collector efficiency under this condition is still above 90%.

3. Load Coupling and Harmonic Suppression

As was preveously mentioned the output of the amplifier may go to a coupling network prior to the load. This network is to match the output impedance of the circuit to the load and also act as a lowpass filter to reduce the harmonic content of the output signal. The specific load coupling network design considerations are given in reference [20].

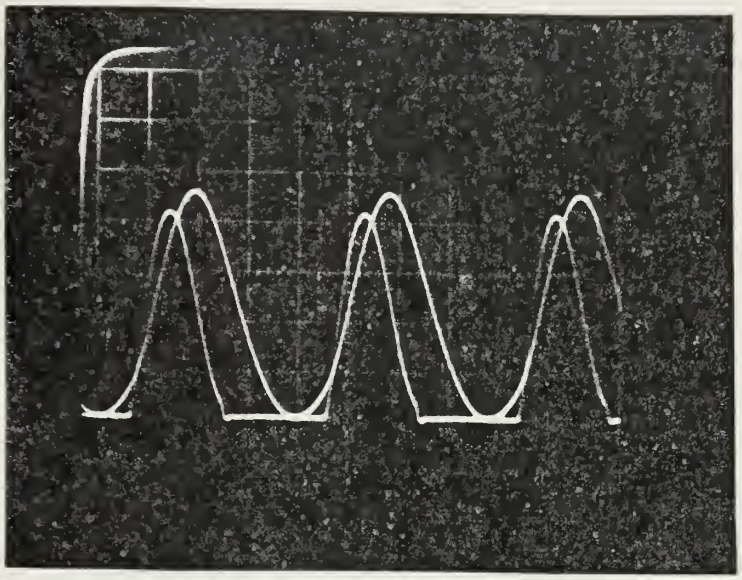
A pi-coupling network was used in the model circuit. It was adjusted to match the output impedance to a 52 ohm

load. This particular coupling network has the advantage of better harmonic suppression characterstics due to the shunt-capacitive arms. The design procedures for this type of impedance transforming network are found in reference [21]. Essentially this network is considered as two back to back L-networks and after calculating the input and output L-sections the series elements are combined to form the pi-network.

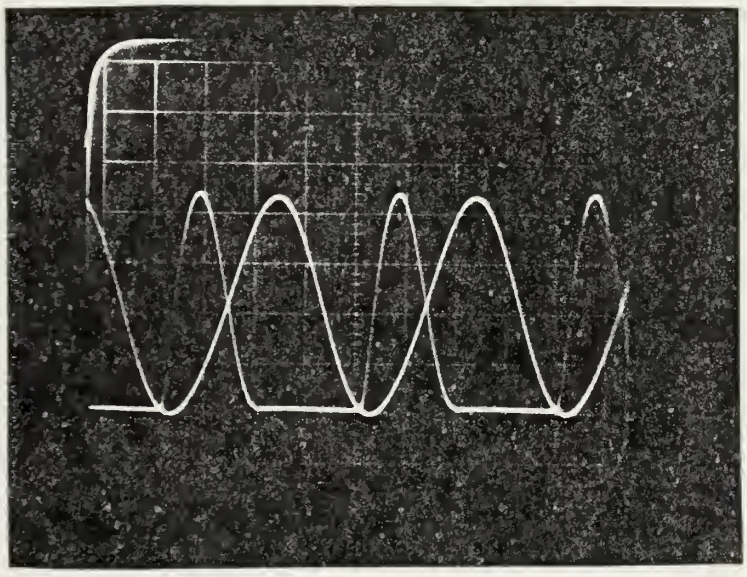
Figure 13 shows the output and collector voltage waveforms, with and without the pi-network. The output using the pi-network is shifted some in phase but is a better sinusoid and the harmonic content is reduced.

E. RECENT DEVELOPMENTS

Until 1976, whenever an application required a high voltage, high current, active device the automatic choice was a bipolar device. Recently a new processing technology has resulted in the development of vertically structured, field effect power devices in which the main current flow occurs in a vertical direction. Several power MOS structures are under development but so far only one such structure is commercially available. These devices can handle up to 25 watts and switch currents up to 2 amperes. They are available with typical 'on' resistances between 1.4 and 3.4 ohms and breakdown voltage ratings between 35 and 90 volts, [22]-[23].



(a) Without pi-network.



(b) With pi-network.

Figure 13 - OUTPUT AND COLLECTOR VOLTAGE WAVEFORMS WITH AND WITHOUT PI-NETWORK. Sinusoid is output voltage. Scale settings: Vc 10 v/div. ; Vo 5 v/div. Horizontal .5 usec./div.

Some of the characterstics of the VMOS device which are improvements over the bipolar device are: 1) Higher input impedances over the entire frequency range; 2) Lower drive currents; 3) Switching speed is only limited by associated circuit capacitance. VMP-1 can switch 1 ampere into a 50 ohm load in 4 nanoseconds.; 4) VMOS does not suffer from thermal runaway; 5) VMOS is free from secondary breakdown; 6) Large values of current gain.

The device also has an unwanted characterstic, its saturation voltage is fairly high (about 10 volts is required at the gate for maximum drain current). However the low current drive requirements offset this disadvantage.

Two factors point to the suitability of VMOS devices for amplifiers. First, the high constant transconductance exhibited for drain currents above approximately 400 milliamperes indicates a potentially more linear performance than can be achieved by a bipolar device. Second, the fast switching speed capability indicates an excellent high frequency characterstic. These two factors as well as the capability to operate in the pulsed mode indicate that this device should find excellent application in high efficiency switching mode amplifiers.

FREQ. KHz.	LOAD POWER WATTS	% DETUNED	COLLECTOR EFFICIENCY
600	0.491	20	83.3
590	0.534	18	85.8
580	0.600	16	86.6
570	0.652	14	87.9
560	0.743	12	90.1
550	0.810	10	91.9
545	0.860	9	92.0
540	0.912	8	92.6
535	0.964	7	91.8
530	1.074	6	93.4
525	1.132	5	92.5
520	1.191	4	92.7
515	1.288	3	94.0
510	1.376	2	94.5
505	1.441	1	95.0
500	1.576=	0	95.7
495	1.602	-1	93.6
490	1.714	-2	94.3
485	1.734	-3	92.7
480	1.772	-4	92.9
475	1.801	-5	92.1
470	1.831	-6	91.8
465	1.854	-7	90.8
460	1.831	-8	88.5
455	1.801	-9	85.0
450	1.772	-10	84.3
440	1.714	-12	80.9
430	1.658	-14	78.0
420	1.575	-16	74.3

Table II - DETUNING EFFECTS ON COLLECTOR EFFICIENCY.

IV. CONCLUSIONS

The class E switching mode rf power amplifier has many advantages over preveously developed amplifiers, the most outstanding being the high overall efficiency obtained with a collector current conduction angle of 180 degrees. Other advantages are: 1) Low stress on the power output transistors, therefore high reliability and low maintenance requirements; 2) Because of the high efficiency, small size and light weight of batteries and heat sinks in portable equipment and low power consumption for high power fixed equipment; 3) Explicit 'a priori' designability.

The development of the class E amplifier, with the advent of VMOS technology, should move the power amplifier from the black box at the end of the block diagram to a circuit which will permeate through the entire design of the equipment.

LIST OF REFERENCES

1. F. E. Terman, Radio Engineering, 3rd Ed. New York: McGraw-hill, 1947, pp. 374-393.

2. J. A. G. Slatter, 'An approach to the Design of Transistor Tuned Power Amplifiers,' IEEE Trans. Circuit Theory, Vol. CT-12, pp. 206-211, June 1965.

3. R. G. Harrison, 'A Nonlinear Theory of Class C Transistor Amplifiers and Frequency Multipliers,' IEEE J. Solid-State Circuits, Vol. SC- 2, pp. 93-102, Sept. 1967.

4. M. R. Osborne, 'Design of Tuned Transistor Power Amplifiers,' Electron. Eng., pp. 436-443, Aug. 1968.

5. R. D. Peden, 'Charge-driven HF Transistor-Tuned Power Amplifier,' IEEE J. Solid-State Circuits, Vol. SC-5, pp. 55-63, Apr. 1970.

6. M. A. H. El-Said, 'Analysis of Tuned Junction-Transistor Circuits Under Large Sinusoidal Voltages in the Normal Domain-Part 1: the Effective Hybrid-Pi Equivalent Circuit,' IEEE Trans. Circuit Theory, Vol. CT-17, pp. 8-12, Feb 1970.

7. -, 'Analysis of Tuned Junction-Transistor Circuits Under Large Sinusoidal Voltages in the Normal Domain-Part 2: Tuned Power Amplifiers and Harmonic Generators,' IEEE Trans. Circuit Theory, Vol. CT-17, pp. 13-18, Feb. 1970.

8. R. H. Johnson and A. r. Boothroyd, 'High Frequency Transistor Frequency Multipliers,' IEEE J. Solid-State Circuits, Vol. SC-7, pp. 81-89, Feb. 1972.

9. N. S. Fuzik, E. A. Sadykov, and V. I. Serguchev, ' Electrical Design of the Oscillatory Circuits of the Final Stage of a Radio Transmitter Operating in the Biharmonic Mode,' Radio Eng., Vol. 25, No. 1, pp. 141-145, 1970.

10. N. S. Fuzik,' Biharmonic Modes of a Tuned RF Power Amplifier,' Radio Eng., Vol. 25, No. 7, pp. 117-124, 1970

11. D. M. Snider, ' A Theoretical Analysis and Experimental Confirmation of the Optimally Loaded and Overdriven RF Power Amplifier,' IEEE Trans. Electron Devices, Vol. ED-14, pp. 851-857, Dec. 1967

12. W. J. Chudobiak and D. F. Page, ' Frequency and Power Limitations of Class D Transistor Amplifiers,' IEEE J. Solid-State Circuits, Vol. SC-4, pp. 25-37, Feb. 1969

13. D. F. Page, W. D. Hindson, and W. J. Chudobiak, ' On Solid-State Class D Systems,' Proc. IEEE (corresp), Vol. 53, pp. 423-424, Apr. 1965

14. P. E. Rose, 'Notes on Class D Transistor Amplifiers,' IEEE J. Solid-State Circuits (corresp.), Vol. SC-4, pp. 178-179, June 1969

15. D. R. Lohrmann, 'Boost Class D Amplifier Efficiency,' Electron. Des., Vol. 16, pp. 96-99, Jan. 4, 1964

16. P. Senak, ' Amplitude Modulation of the Switched-Mode Tuned Power Amplifier,' Proc. IEEE, Vol. 53, No. 10, pp. 1658-1659, Oct. 1965

17. G. D. Ewing, High Efficiency Radio Frequency Power Amplifiers, Ph.D Thesis, Oregon State University, 1964

18. N. O. Sokal and A. D. Sokal, ' Class E- A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers,' IEEE J. Solid-State Circuits,Vol. SC-10, No. 3, pp. 168-176, June 1975

19. R. H. Raab, 'High-Efficiency Amplification Techniques,' IEEE Trans. Circuits and Systems, Vol. 7, No. 10, pp. 3-11, Dec. 1975

20. N. O. Sokal and F. H. Rabb, 'Harmonic Output of Class E RF Power Amplifiers and Load Coupling Network Design,' IEEE J. Solid-State Circuits (corresp.), Vol. SC-12, No. 1, pp. 86-88, Feb. 1977

21. Reference Data for Radio Engineers, 6th ed., pp. 7.1-7.20, ITT, 1975

22. 'Siliconix Technical Article TA76,' November 1976

23. 'Siliconix Technical Article TA76,' August 1976

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